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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,905	11/05/2003	Brent A. Anderson	BUR920030098US1	2904

30449 7590 04/14/2005

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,905	ANDERSON ET AL.	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *22-28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/05/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of claims 1-21 in the reply filed on 02/10/2005 is acknowledged. The traversal is on the ground(s) that the subject matter of all the claims is sufficiently related that a thorough search of all the claims could be made without serious burden on the examiner. This is not found persuasive because although the subject matter of all the claims is related, a thorough search of two separate and distinct inventions can not be made without serious burden on the examiner.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-4, 8 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin et al. (6,852,576).

Lin et al. teach in figures 1-9 and related text a method of forming an FinFET device, comprising:

(a) providing a semiconductor substrate 200,

(b) forming a dielectric layer on a top surface of said substrate (column 3, lines 6-8);

(c) forming a silicon fin 410 on a top surface of said dielectric layer;

(d) forming a protective layer 510 on at least one sidewall of said fin; and

(e) removing said protective layer from said at least one sidewall in a channel region of said fin (column 4, lines 7-8).

(f) forming a gate dielectric on exposed surfaces of said fin in said channel region; and

(g) forming a conductive gate on said gate dielectric.

(h) removing said protective layer from source/drain regions of said fin,

wherein said fin has a height of about 500 to 2000A and has a width of about 200 to 500A, and wherein said fin comprises mono-crystalline silicon.

Claims 11-13, 15-16 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Yeo et al. (6,867,433).

Yeo et al. teach in figure 12 and related text a method of forming an FinFET device, comprising:

(a) providing a semiconductor substrate 204,

(b) forming a dielectric layer 152 on a top surface of said substrate;

(c) forming a silicon fin 155 having sidewalls on a top surface of said dielectric layer;

(d) forming a protective spacer layer 164 on at least one sidewall of said fin; and

(e) performing at least one ion implantation step into said fin.

(f) forming a gate dielectric 164 on exposed surfaces of said fin in said channel region;

(g) forming a conductive gate 1610 on said gate dielectric,

wherein said protective layer comprises tetraethoxysilane oxide or silicon nitride, and is about 15 to 50A thick,

wherein step (c) comprises: forming a silicon layer 202 on said top surface of said dielectric layer 152 (figure 12a); forming a mask (not shown) over said silicon layer; removing portions of said silicon layer not protected by said mask to expose said dielectric layer; and removing said mask.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

Claims 2, 6-7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view Yeo et al.

Regarding claim 9, Lin et al. teach substantially the entire claimed structure, as applied to claim 1 above, except disclosing the method of forming the silicon fin.

Yeo et a. teach forming the silicon fin by forming a silicon layer 202 on said top surface of said dielectric layer 152 (figure 12a); forming a mask (not shown) over said silicon layer; removing portions of said silicon layer not protected by said mask to expose said dielectric layer; and removing said mask. It would have been obvious to a person of

ordinary skill in the art at the time the invention was made to form the silicon fin by forming a silicon layer on said top surface of said dielectric layer and forming a mask over said silicon layer; removing portions of said silicon layer not protected by said mask to expose said dielectric layer; and removing said mask in Lin et al.'s device in order to simplify the processing steps of making the device by using conventional masking and etching process.

Regarding claim 2, prior art teaches forming at least one ion implantation step into said fin. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include between steps (d) and (e) performing at least one ion implantation step into said fin in Lin et al.'s device in order to have better control over the ion implantation of the device.

Regarding claims 6 and 7, Yeo et al. teach a protective layer comprises tetraethoxysilane oxide or silicon nitride, and is about 15 to 50A thick. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a protective layer comprises tetraethoxysilane oxide or silicon nitride, and is about 15 to 50A thick in Lin et al.'s device in order to improve the device characteristics by using silicon nitride insulating layer.

Claims 17 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeo et al. in view Lin et al.

Regarding claims 17 and 21, Yeo et al. teach substantially the entire claimed structure, as applied to claim 1 above, except said fin has a height of about 500 to 2000A and has a width of about 200 to 500A, and wherein said fin comprises mono-crystalline silicon. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form said fin having a height of about 500 to 2000A and a width of about 200 to 500A, and wherein said fin comprises mono-crystalline silicon in Yeo et al.'s device in order to reduce the size of the device and in order to improve the device characteristics.

Regarding claims 19 and 20, Lin et al. teach in figures 2-4 step (c) comprises: forming a mandrel 210 on said dielectric layer, depositing a conformal silicon layer 310 on a top surface and a sidewall of said mandrel and on surfaces of said dielectric layer not covered by said mandrel, removing said conformal silicon layer from said top surface of said mandrel and said surfaces of said dielectric layer not covered by said mandrel, and after the step of removing, performing a high temperature anneal of said conformal silicon layer. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form step (c) by the process of Lin et al.'s in Yeo et al.'s device in order to improve the device characteristics.

Claims 5 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeo et al. or Lin et al. in view of Buynoski et al. (6,709,982).

Yeo et al. or Lin et al. teach substantially the entire claimed structure, as applied to claim 1 above, except removing a portion of said dielectric layer from under said fin in a step between steps (c) and (d). Buynoski et al. teach in figures 6-7 removing a portion 620 of said dielectric layer 210 from under said fin 720 in a step between steps (c) and (d). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to remove a portion of said dielectric layer from under said fin in a step between steps (c) and (d) in the process of forming the device of Lin et al. or Yeo et al. in order to obtain a FinFET with improved device characteristics.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References D-E are cited as being related to FinFET's.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722

and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
4/11/05

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800